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Semiconductor fabrication techniques for producing an ultra-flat reflective slit

Thomas E. Vandervelde[a,b], Michael J. Cabral[c], John Wilson[a], Michael Skrutskie[*a]
[a]Astronomy Department, University of Virginia, 530 McCormick Road, Charlottesville, VA 22904
[b]Coordinated Science Laboratory, University of Illinois Urbana-Champaign, 1308 West Main Street, Urbana, IL 61801
[c]Charles L. Brown Department of Electrical and Computer Engineering, University of Virginia, 351 McCormick Road, Charlottesville, VA 22904

Abstract

The most difficult aspects in manufacturing a reflective slit substrate are achieving a precisely fabricated slit surrounded by an optically flat surface. Commonly used fabrication techniques include polishing a metal substrate that has a slit cut by electric discharge machine (EDM) methods. Another common method is to deposit a reflective coating (with a slit masked-off) via photolithography onto a glass or crystalline substrate. Here, we present a departure from these traditional methods and employ the advantages inherent in integrated circuit fabrication. By starting with a silicon wafer, we begin with a nearly atomically flat surface. In addition, the fabrication tools and methodologies employed are traditionally used for high precision applications: this allows for the placement and definition of the slit with high accuracy. If greater accuracy in slit definition is required, additional tools, such as a focused ion beam, are used to define the slit edge down to tens of nanometers. The deposition of gold, after that of a suitable bonding layer, in an ultra-high vacuum chamber creates a final surface without the need of polishing. Typical results yield a surface RMS-roughness of < 2nm. Most of the techniques and tools required for this process are commonly available at research universities and the cost to manufacture said mirrors is a small fraction of the purchase price of the traditional ones.

Keywords: Reflective slit, lithography, silicon, semiconductor processing

Introduction

In recent decades, advancing semiconductor fabrication techniques have been required to keep pace with Moore's Law. Precision lithography and epitaxial techniques have enabled researchers to define structures nanometers in size and deposit layers of material one-atom thick. These techniques have been employed towards making better semiconductor devices for use in astronomy and other fields (e.g. photodetectors). They have also been used to produce silicon gratings, immersion gratings and grisms (see e.g. Keller et al. 2000, Keller et al. 2002 and Ge et al. 2003) as well as pupil masks. In this paper, we discuss an additional dissemination: slit mirrors.

Slit Mirrors have been used in astronomical instruments at various wavelengths. We use the term `slit mirror' to mean an optic with a reflective surface except in certain areas which allow light to pass through apertures such as rectangular shaped slits; alternatively, the aperture could just as well have different shape, such as a circular hole. The apertures generally serve as entrance slits for a spectrograph. Light that does not go through the slit is reflected into other optical paths, such as a slit viewer or guide camera.

One method for fabricating slit mirrors has been to deposit a reflective coating onto a polished glass or crystal substrate. The area of the slit is masked off through various means during the coating process. This method gives a reflective surface with tight surface figure tolerances through traditional polishing methods. In addition, the edges of the slit can be defined to high accuracy through lithographic techniques. While this slit is precisely defined, the light that goes through it suffers throughput losses owing to crossing the two refractive surfaces of the substrate. SpeX on the IRTF (Rayner et al. 2003) uses CaF2 slit mirrors with reflective coatings applied lithographically.

[*] Skrutskie@virginia.edu; phone 1 434 924-4328; fax 1 434 924-3104; astro.virginia.edu

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An alternative method is to manufacture a so-called `air slit' to avoid the throughput losses just mentioned. These can be manufactured by cutting a slit in a metal substrate using precision machining methods such as wire electric discharge machining (wire-EDM). The metal surface can be polished to high surface accuracy before or after cutting the slit using for instance diamond machining. EDM machining can also be used to remove material from the back of the substrate near the slit to create slit `jaws'. While this technique is precise by machining standards, it does not reach the level of accuracy inherent in the lithography-based technique. The Infrared Camera and Spectrograph (IRCS) on the Subaru telescope uses tungsten-carbide slit mirrors machined with wire-EDM (Young et al. 1998). The IRCS slit mirrors were specified to have 0.8 μm slit edge roughness and 3 nm surface roughness. Air slits have also been manufactured using electroforming techniques; e.g. the slit apertures for the Space Telescope Imaging Spectrograph (STIS; Woodgate et al. 1998). Lastly, air slits with widths as small as 10 μm and sub-micron straightness have been manufactured by diamond machining (Comstock et al. 2006).

Given the inherent atomic flatness of silicon wafers, it occurred to us to investigate the manufacture of slit mirrors using silicon-processing techniques. These techniques include the ability to deposit extremely smooth layers of gold or other reflective metals into precisely defined regions and to etch slits through a wafer with nanometer precision. This seemed advantageous because we would be able to use lithography techniques to precisely define the slit, as was done in the first process above, while generating an 'air slit' via precision dry/wet etching to eliminate the refractive surfaces, thereby potentially receiving the benefits of both present designs.

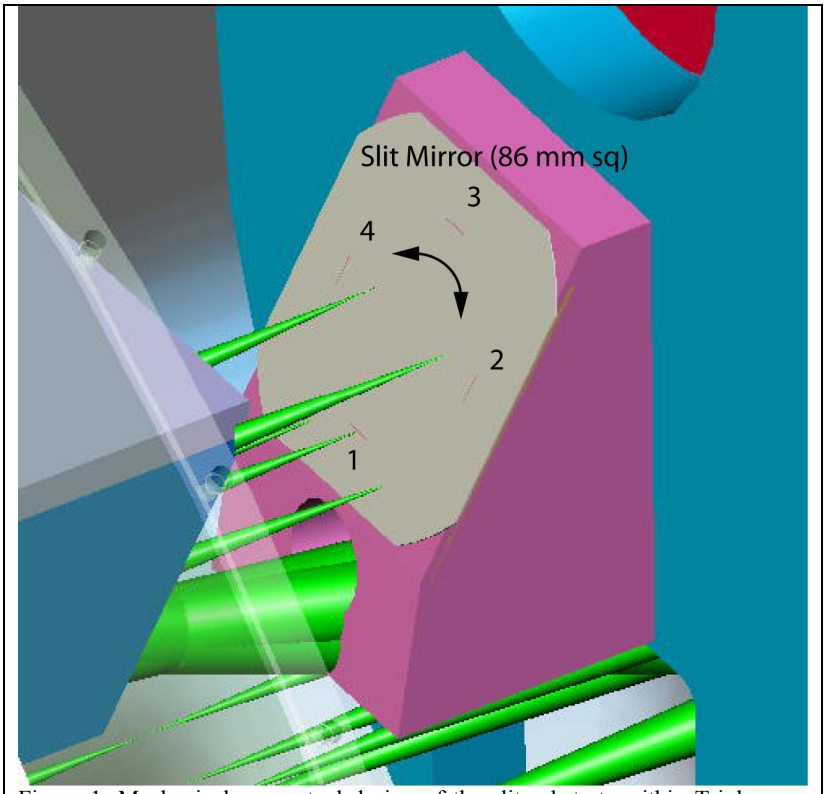

Figure 1: Mechanical conceptual design of the slit substrate within Triplespec. Light that falls on the slit at position 1 passes into the spectrograph train of the instrument. Light that falls elsewhere on the slit mirror is reflected up and to the left (in the sense of the figure) into a separate slit viewing channel (not shown). A cryogenic motor will rotate the slit mirror to allow selection of slits with various widths.

The University of Virginia is collaborating with Cornell, JPL and Caltech to build three near-identical copies of a moderate-resolution (R~3000) near-infrared spectrograph (Wilson et al. 2004). Cornell and JPL are teaming to build a copy for the Palomar 200-inch. Caltech is building a copy for the Keck 10-m. Additionally, the University of Virginia copy will go on the Apache Point Observatory 3.5 m. The spectrograph design includes a reflective slit mirror: light that does not go through the slit is reflected into an optical train that reimages the telescope focus in the K_s photometric band (2.16μm) to provide near-infrared slit-viewing and guiding. We desired a slit substrate with four slits of varying slit widths. The slit substrate will be rotated to choose the desired slit based on science requirements and seeing (see Figure 1).

Methodology

Our technique varies from the traditional air-slit process in a fundamental way: previously, one started with inherently rough material and tried to smooth it to a suitable polish, whereas with our lithography based process we begin with a silicon wafer, which is effectively atomically flat, and try to minimize any induced roughness. In the most basic terms, our process can be broken down into three phases: First, we pattern and etch the slits most of the way

through the wafer from the backside, while protecting the front side. Second, pattern and etch the slits the rest of the way through the wafer from the front side to achieve a high degree of precision in the slit placement and definition. Third and lastly, we deposit the reflective gold coating on the front side of the wafer.

Before patterning can be accomplished, two chrome-on-quartz photomasks must be designed and fabricated. The design of the photomask for the frontside of the mirror is straightforward. It consists of four slits of various widths spaced equally from the center, as shown in Figure 1. The design of the backside mask is not as straightforward, however. While the locations of the backside slits are the same as for the frontside mask, the dimensions of the slits themselves are quite different. The dimensions of the backside slits are dependent on two factors: frontside slit dimensions and wafer thickness. Because an anisotropic etch is used for removing material from the backside of the wafer, the dimension of the backside slit will be much larger than that of the frontside slit width. Once the wafer thickness is measured, the backside slit width can be calculated using:

$$backside\ slit\ width = frontside\ slit\ width + 2\left(\frac{wafer\ thickness - X}{\tan(54.7)}\right)$$

where X is the silicon thickness that is not etched. This equation is valid when using a (100) silicon wafer, since the angle between the fast etching (100) plane and the slow etching (111) plane is 54.7°.

After the photomasks have been designed and fabricated, it is necessary to prepare the wafer for patterning. Since the majority of the etching will be done via wet chemistry, a protective hard mask must be deposited on both sides of the double-polished silicon wafer. Thermally grown silicon dioxide has a sufficiently low etch rate in the anisotropic etch, so it can be used. For our process, the wafer is placed into an oxide furnace at 1100°C, with water vapor flowing into the quartz tube. After 80 minutes, the wafer is removed and the silicon dioxide thickness is measured at approximately 660nm using an optical measurement tool.

With a sufficiently thick etch mask in place on the wafer, the wafer is patterned. First, the backside is cleaned on a spinner using ethanol, D-limonene, and methanol, followed by a 5-minute dehydration bake at 120°C. Next, AZ5214E image reversal photoresist is spun onto the backside of the wafer at 6000rpm for 30 seconds. After a short pause, a soft-bake is performed at 100°C for 2 minutes. The backside of the wafer is now ready to be lithographically defined. The wafer is first exposed to a UV light source for 30 seconds through the

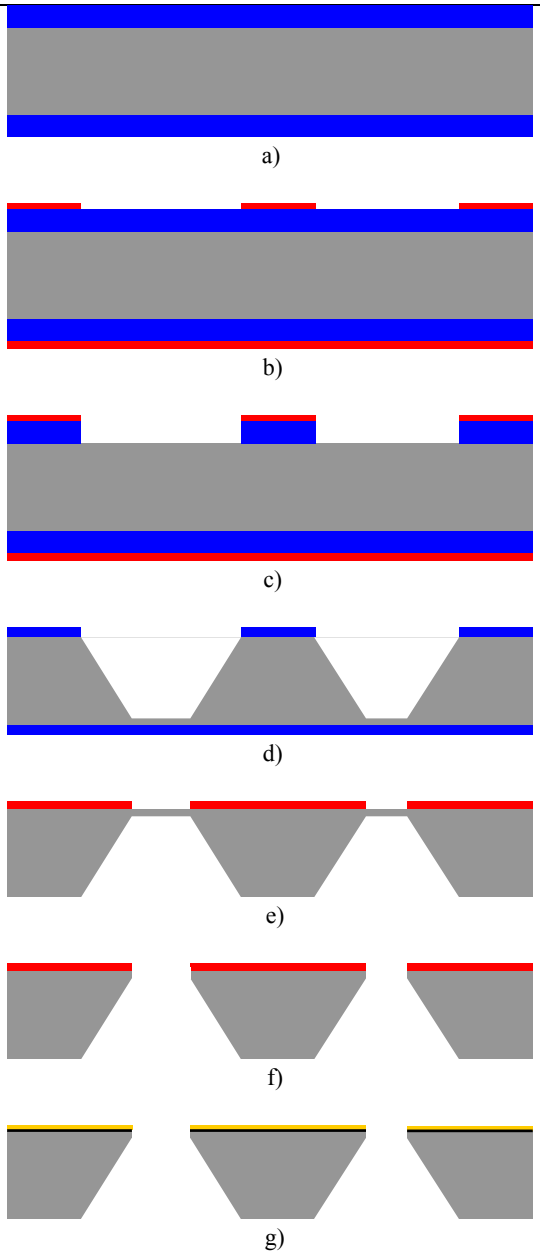

Figure 2: The Fabrication Process – a) Thermally oxidize a doubly polished (100) Si wafer. b) Pattern photoresist on backside of wafer (top). Coat frontside of wafer (bottom) with photoresist. c) Using a wet etch (BOE), remove the exposed silicon dioxide. d) After removing the photoresist, anisotropically etch the silicon wafer. Ensure that the etch does not reach the silicon dioxide on the frontside of the wafer. e) Remove the remaining silicon dioxide from both sides of the silicon wafer. Pattern the frontside of the wafer with photoresist. f) Using a reactive ion etch (dry etch), etch the exposed silicon surface. g) Remove the photoresist. Coat the frontside of the wafer with Au(100nm)/Ti(5nm).

backside photomask. Then, the image-reversal property of the AZ5214E photoresist is utilized with a 100°C bake followed by a flood (no photomask) UV exposure for 50 seconds. Once exposed, the photoresist is developed in a solution of AZ400K 1:4 developer for approximately 20 seconds. After verifying the pattern transfer with a microscope, the front side of the wafer is coated with AZ5214E photoresist. No patterning of this photoresist layer is done, it is only used to protect the silicon dioxide layer on the front of the wafer.

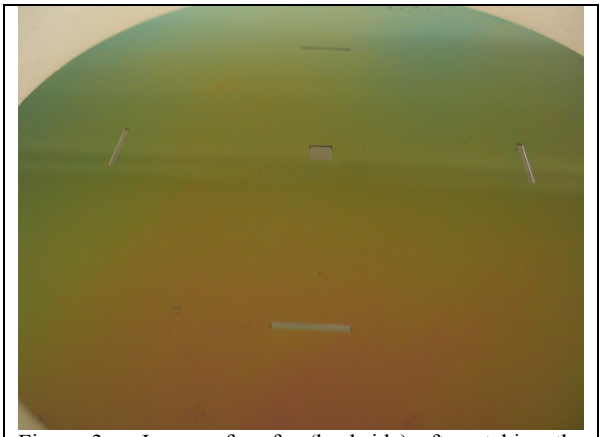

Figure 3: Image of wafer (backside) after etching the backside in 1:1::KOH(45%):DI. Four slits and a center square for attachment to a rotational shaft are visible. Note: Disk shown is a four-inch wafer.

With the entire wafer coated with photoresist, except for the 4 slits and a central square on the backside, the wafer is placed into a Buffered Oxide Etch (BOE) solution of 10 parts Ammonium Fluoride (40%) and 1 part Hydrofluoric Acid (49%). With a nominal etch rate of 600Å/min, the exposed silicon dioxide is removed after 11 minutes, but the wafer is left in the solution for an additional 1 minute to ensure that all of the oxide layer is indeed removed from the backside slit areas. Upon removal from the BOE etch, the silicon dioxide layer on the back side of the wafer is an exact copy of the backside photomask, and it can be used to transfer the pattern into the silicon wafer itself. Since silicon will oxidize immediately when exposed to atmosphere, the wafer is immediately placed into the anisotropic etch solution after being removed from the BOE solution. The anisotropic etch solution is a heated mixture of 1:1::KOH(45%):H_2O. The exact etch rate of the anisotropic etch solution depends greatly on concentration and temperature. As such, rather than solely relying on a calculated etch time, the wafer is periodically removed from the etch solution and the depth of the slit is measured using an optical profilometer. After the etching has progressed to the point where there are only a few micrometers of silicon remaining in the area of the slit, the wafer is placed into a fresh BOE solution which removes the remaining silicon dioxide from both the front and back of the wafer.

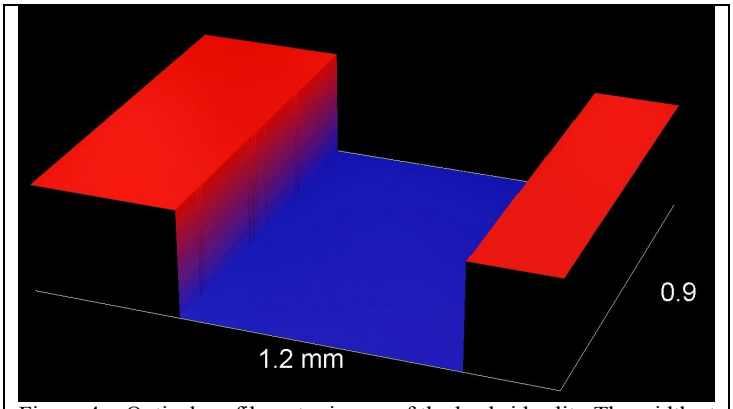

Figure 4: Optical profilometer image of the backside slit. The width at the top of the slit is 652um, and the edge roughness is sub-micron. Walls slope inward at a 55° angle.

With the majority of the air-slit defined through anisotropic etching from the back side, the final patterning and etching step is performed on the front side of the wafer. Since the backside is already etched, the front side pattern must be aligned to the backside slits. For this, a back-side alignment process is used. This means that all of the alignment, which is normally done from the top, through the transparent photomask, must instead be done from underneath the wafer. First, the front-side photomask is loaded into the aligner and an image is taken of its location. Then, the wafer, which has photoresist spun onto its frontside, is loaded with the already etched side facing downward, away from the photomask. Real-time images are taken of the wafer and compared against an overlay of the front-side photomask image. By adjusting the wafer position, the slits from the front-side photomask can be aligned within 2 μm so that they fall within the slits fabricated by the backside patterning and etching. Once the wafer is aligned properly, it is exposed to UV light through the front-side mask. The photoresist is then developed and the pattern transfer is inspected with a microscope.

The wafer is placed, photoresist side up, into a Reactive Ion Etching (RIE) tool. The highly anisotropic etching tool uses an SF_6 based plasma to etch the remaining exposed silicon, completing the fabrication of the air-slit through the silicon wafer. RIE is used for this final step because of its ability to produce extremely sharp edges and high aspect ratios. This step is the one that actually defines the slit dimension for the incoming light, so the extreme precision is warranted here. After the silicon etch is complete, the photoresist is removed with an O_2 plasma followed by a methanol rinse, and the wafer is loaded into an electron-beam evaporator. After pumping the evaporator chamber to a pressure near $5x10^{-7}$ Torr, an adhesion layer of 5 nm of Ti is deposited onto the front-side of the wafer at a rate of 1 Å/second. The Ti film is followed by a 100 to 200 nm layer of Au evaporated at 10 Å/second. The wafer is taken from the evaporator, mounted to a carrier wafer with Apiezon wax and cut, using a dicing saw, into the final desired dimension. Upon removal from the carrier wafer, the slit substrate is complete and ready for installation.

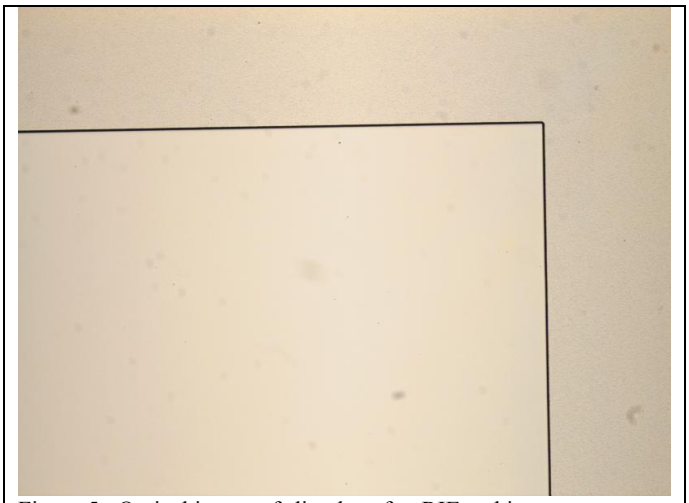

Figure 5: Optical image of slit edge after RIE etching.

Results

Using the procedure outlined in this paper, we were able to fabricate precisely defined and placed slits. Figure 3 is an optical picture of the backside of the wafer after patterning and anisotropic etching. The four slits and a center square (to be used for attachment to a rotational shaft) are visible. This process creates an opening with an angle of 54.7 degrees, see Figure 4. Having a slit that angles outwards was desired for our configuration, but the substitution of [100] silicon wafers with [110] silicon wafers would generate slit walls normal to the surface if that is desired. Inspection of the slit edges after anisotropic etching, as illustrated in Figure 6, shows that the slit edge roughness is less than 50nm, much less than that required for our application. The RIE etching step leaves a clean sharply defined line, as shown in Figure 5; thereby, completing the 'air gap' in the slit. After completely etching through the wafer, closer examination of the slit edge shows that it remains very smooth, as illustrated in Figure 7. After the slits were etched, the Au/Ti coating was deposited onto the wafer and the surface roughness was determined to be < 2nm (Figure 8).

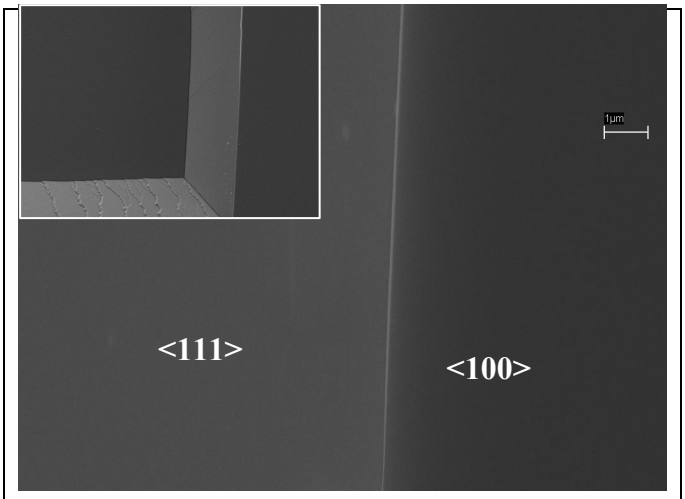

Figure 6: SEM image of Si slit roughness after anisotropic etching (marker is 1µm). Inset Depicts a zoomed out image of the interface.

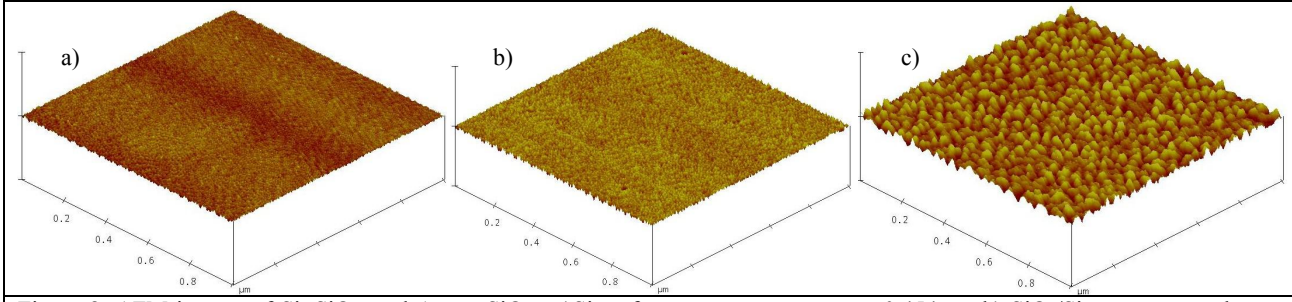

Figure 8: AFM images of Si, SiO_2, and Au on SiO_2. a)Si surface; average rougness = 0.454nm. b) SiO_2/Si; average roughness = 0.708nm c) Au(100nm)/Ti(5nm)/SiO_2/Si; average roughness = 1.46nm

Conclusions

In this paper, we have detailed a process to make slit mirrors using semiconductor fabrication techniques available at most universities. These slit mirrors have < 2nm surface roughness achieved without polishing, slit dimensions defined within nanometers, and slit edge roughness < 50 nm, which compare well with slit mirrors produced via traditional macro-machining techniques. If desired, additional semiconductor fabrication techniques can be used to reduce the surface roughness further and more precisely define the slits to enable the extension of slit mirror technology to smaller wavelength detectors.

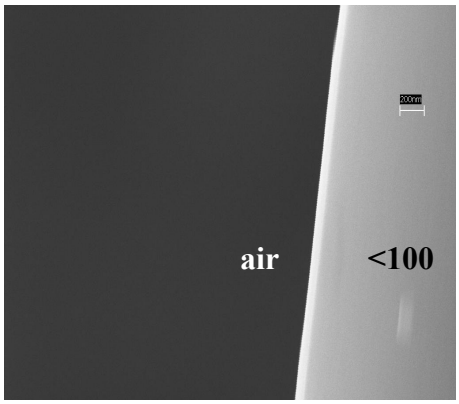

Figure 7: SEM image of slit edge after the air slit is fabricated (marker is 200nm)

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